Amendments to the Claims

This listing of the claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-25. (canceled)

26. (previously presented): A decoder system, comprising:

an address input for receiving an address signal representing any of a plurality of address values (D);

a plurality of intermediate nodes;

a decoder responsive to the address signal and arranged to stimulate, for each address value, a respective combination of the intermediate nodes; and

a plurality of outputs, each responsive to a respective group of the intermediate nodes such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group;

wherein the decoder is arranged to perform a plural-stage process in determining which of the intermediate nodes to stimulate in response to each address value, said plural-stage process comprising at least a first stage in which results are determined and a second stage for which the results of the first stage are provided as inputs,

wherein the plural-stage process comprises the determination of a word of a predetermined constant weight code.

27. (previously presented): A system as claimed in claim 26, wherein the decoder comprises a microprocessor which is programmed to perform the plural-stage process.

28. (previously presented): A system as claimed in claim 26, wherein the decoder comprises hard-wired logic circuitry and/or arithmetic circuitry and/or look-up circuitry arranged to perform the plural-stage process.

29. (previously presented): A system as claimed in claim 26, wherein the plural-stage process comprises the determination of a word of a predetermined constant weight code.

30. (previously presented): A system as claimed in claim 26, wherein, in response to each address value, a respective single one of the outputs is stimulated, or stimulated beyond a predetermined threshold.

31. (canceled)

32. (currently amended): A method of manufacturing a decoder system having the following elements:

an address input for receiving an address signal representing any of a plurality of address values (D);

a plurality of intermediate nodes;

a decoder responsive to the address signal and arranged to stimulate, for each address value, a respective combination of the intermediate nodes; and

a plurality of outputs, each responsive to a respective group of the intermediate nodes such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group,

wherein the decoder is arranged to perform a plural-stage process in determining which of the intermediate nodes to stimulate in response to each address value, said plural-stage process comprising at least a first stage in which results are determined and a second stage for which the results of the first stage are provided as inputs;

wherein the method of manufacturing comprises ~~the steps of~~:

providing such a decoder which is:

responsive to an address signal representing any of a plurality of address values; and arranged to stimulate, for each address value, a respective combination of intermediate nodes;

providing a plurality of outputs;

determining, for each output, a respective group of the intermediate nodes to which that output is to be responsive; and

rendering each output responsive to the intermediate nodes in the respective determined group such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group;

~~characterised by the steps of:~~

determining a plural-stage process to be performed by a decoder, said plural-stage process comprising at least a first stage in which results are determined and a second stage for which the results of the first stage are provided as inputs;

arranging the decoder to perform the determined plural-stage process in determining which of the intermediate nodes to stimulate in response to each address value; and

using the determined plural-stage process in said step of determining the group of the intermediate nodes to which the outputs are to be responsive.